Letter

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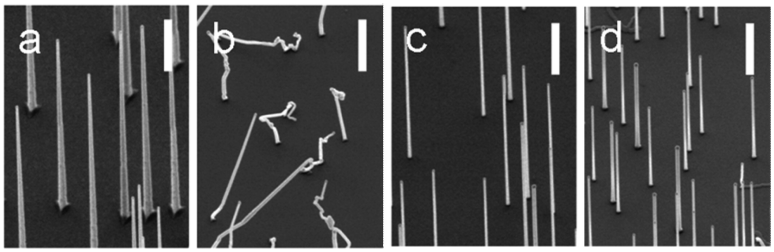

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Twin-Free Uniform Epitaxial GaAs Nanowires Grown by a Two-Temperature Process

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ABSTRACT

We demonstrate vertically aligned epitaxial GaAs nanowires of excellent crystallographic quality and optimal shape, grown by Au nanoparticle-catalyzed metalorganic chemical vapor deposition. This is achieved by a two-temperature growth procedure, consisting of a brief initial high-temperature growth step followed by prolonged growth at a lower temperature. The initial high-temperature step is essential for obtaining straight, vertically aligned epitaxial nanowires on the (111)B GaAs substrate. The lower temperature employed for subsequent growth imparts superior nanowire morphology and crystallographic quality by minimizing radial growth and eliminating twinning defects. Photoluminescence measurements confirm the excellent optical quality of these two-temperature grown nanowires. Two mechanisms are proposed to explain the success of this two-temperature growth process, one involving Au nanoparticle–GaAs interface conditions and the other involving melting–solidification temperature hysteresis of the Au–Ga nanoparticle alloy.

Semiconductor nanowires have attracted considerable research interest in recent years as potential nanobuilding blocks for future electronic and optoelectronic devices. Nanowire lasers,[1,2] photodetectors,[3] field-effect transistors,[4] and single-electron memory devices[5] have already been demonstrated. Free-standing III−V nanowires, including axial and radial heterostructure nanowires, hold great promise.

Metalorganic chemical vapor deposition (MOCVD) is commonly used to grow epitaxial III−V nanowires on III−V substrates, according to a Au nanoparticle-catalyzed vapor−liquid−solid or vapor−solid−solid process.[6,7] The properties of these CVD-grown nanowires are highly sensitive to growth temperature. Higher temperatures induce significant radial overgrowth, manifested as nanowire tapering,[6,8] undesirable shell structures in axial heterostructure nanowires,[9] and compositional nonuniformity along the length of ternary nanowires.[10] Furthermore, recent studies have shown that the density of crystallographic defects increases with growth temperature.[11] At lower temperatures, however, nanowire growth becomes unstable and prone to kinking and does not exhibit perfect epitaxy with the substrate.[12,13] These growth issues must be controlled because device applications demand straight, well-oriented epitaxial nanowires with uniform diameters, controllable composition, and good crystallographic and optoelectronic properties.

We have devised a two-temperature procedure for optimum GaAs nanowire growth. Such a procedure has previously been investigated for Ge nanowires.[13,14] Growth begins with a brief high-temperature "nucleation" step, necessary for epitaxial nucleation and growth of straight, vertically aligned nanowires on the (111)B GaAs substrate. This is followed by a prolonged "growth" step at a lower temperature. Without the prior nucleation step, such a low growth temperature would produce nonvertical, kinked, and irregular nanowires. The low growth temperature minimizes radial growth and tapering. Significantly, transmission electron microscopy (TEM) studies reveal that the low growth temperature yields nanowires that are free of planar crystallographic defects, in marked contrast to the high density of twinning defects found in nanowires grown at higher temperatures. Photoluminescence (PL) measurements reveal

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the excellent optical quality of nanowires obtained by this two-temperature procedure.

Nanowires were grown on semi-insulating GaAs (111)B substrates. Substrates were functionalized by immersion in 0.1% poly-L-lysine (PLL) solution, rinsed in deionized water, and treated with Au colloid solution containing 50 nm diameter Au nanoparticles (4.5×10^{10} nanoparticles/mL). The nanoparticles are attracted to, and immobilized on, the PLL layer. Nanowires, catalyzed by these nanoparticles, were grown by horizontal flow MOCVD at a pressure of 100 mbar and a total gas flow rate of 15 slm. Prior to growth initiation, the substrate was annealed in situ at 600 °C under AsH_3 ambient to desorb surface contaminants. After cooling to the desired temperature, trimethylgallium (TMG) was introduced to initiate nanowire growth by either a single-temperature or two-temperature procedure. The single-temperature procedure involved 30 min of growth at a constant temperature, T_g, between 350 and 450 °C. For the two-temperature procedure, growth initiated with a 1 min "nucleation" step at the nucleation temperature, T_n, of 450 °C. The temperature was then rapidly ramped down to the subsequent growth temperature, T_g, between 330 and 390 °C. Total growth time was 31 min, including the nucleation and cooling steps, and typical cooling time was between 2.5 and 6.5 min. Source flows of TMG and AsH_3 were 1.2×10^{-5} and 5.4×10^{-4} mol/min, respectively.

Nanowires were characterized by field emission scanning electron microscopy (FESEM), TEM, and PL measurements. FESEM images were obtained with an accelerating voltage of 3 kV. TEM investigations were carried out using a FEI Tecnai F30. TEM specimens were prepared by ultrasonicating nanowire samples in ethanol for 20 min and then dispersing the nanowires onto holey carbon grids.

For PL measurements, GaAs nanowire cores were grown as described above, then clad in an AlGaAs shell to passivate the GaAs surface.[15,16] AlGaAs shell growth was performed for 20 min at 650 °C, with a trimethylaluminium flow of 4.1×10^{-6} mol/min, and TMG and AsH_3 flows, as described above. Nanowires were transferred from the as-grown substrate to Au-coated Si substrates by gently touching the two substrates together. PL spectra of nanowire ensembles were obtained at 10 K, using the 532 nm line of a frequency-doubled diode-pumped solid-state (DPSS) laser for excitation, with the resulting PL dispersed through a 0.5 m monochromator then detected by a Si photodetector. Microphotoluminescence (micro-PL) images were obtained at room temperature using an epifluorescence microscope (Nikon Eclipse L150). Individual nanowires were excited through a 100×/0.9 NA objective (Nikon CFI LU Plan Epi) using the DPSS laser and the resulting PL was collected through this objective and imaged onto a Peltier-cooled CCD camera (Nikon DS-5Mc).

Nanowires grew within the entire temperature range tested, even at the lowest trialed T_g of 330 °C. Within this temperature range, however, nanowire morphology varied significantly. We focus on the temperature conditions, T_n and T_g, required for high-quality straight [111]B-oriented nanowires.

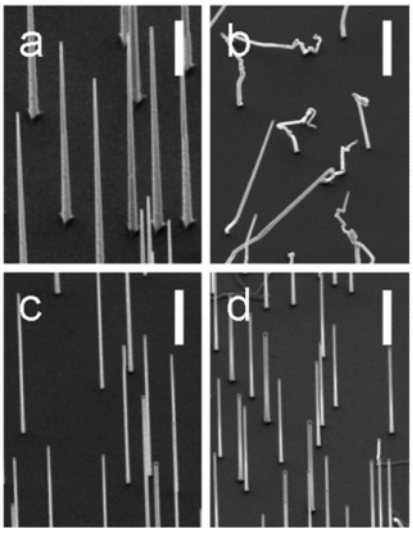

Figure 1. FESEM images of GaAs nanowires grown by single-temperature and two-temperature procedures at various T_g. (a) Single-temperature procedure with T_g of 450 °C. (b) Single-temperature procedure with T_g of 390 °C. (c) Two-temperature procedure with T_g of 390 °C (T_n of 450 °C). (d) Two-temperature procedure with T_g of 350 °C (T_n of 450 °C). Samples are tilted at 40°. Scale bar is 1 μm.

Table 1. Summary of Nanowire Morphology for Single- and Two-Temperature Procedures with Various Growth Temperatures (T_g). Tapering Is Calculated for Straight Nanowires Only

procedure	T_n (°C)	T_g (°C)	straight [111]B nanowires (% of total)	tapering (nm/μm)
1-temperature		450	98	17
1-temperature		390	1	
1-temperature		350	0	
2-temperature	450	390	99	<3
2-temperature	450	350	88	<2
2-temperature	450	330	0	

Figure 1 illustrates FESEM images of nanowires grown by single- and two-temperature procedures at various T_g. Table 1 summarizes key samples, their growth parameters, and the proportions of vertical [111]B-oriented nanowires as determined from counts of over 500 nanowires per sample. Nanowires grown by the single-temperature procedure were generally straight and epitaxially aligned in the vertical [111]B direction when grown at T_g of 410 °C and above (Figure 1a), but suffer severe tapering. At T_g of 390 °C and below (Figure 1b), nanowire growth rarely initiated in the vertical [111]B direction, and subsequent kinking was common: the initial and final nanowire orientations exhibit no apparent relationship with the substrate. In contrast, the two-temperature procedure allowed the growth of straight, vertical [111]B-oriented nanowires at T_g as low as 350 °C (Figure 1c and d), significantly lower than previously reported.[6,17] We determine a minimum T_n of 410 °C, and a minimum T_g of 350 °C are required for this straight epitaxial nanowire growth.

Because there are reports that PLL can affect nanowire growth direction,[18−20] we also prepared substrates without

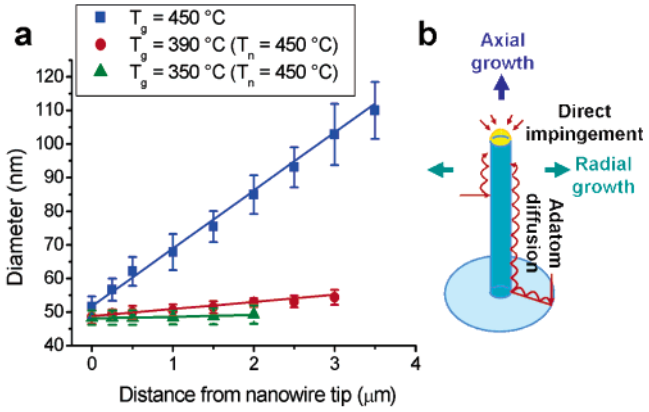

Figure 2. (a) Plot of nanowire diameter measured at distances from the Au nanoparticle−nanowire interface for three T_g. Nanowires were grown by either a single-temperature or a two-temperature procedure, at the indicated T_n and T_g. Error bars represent standard deviations of samples of 10 nanowires at each point. (b) Schematic illustrating axial and radial nanowire growth, fed by direct impingement of precursor species on the nanoparticle and Ga adatom diffusion from the substrate and along nanowire sidewalls.

PLL by allowing a diluted droplet of Au colloid solution (9×10^8 nanoparticles/mL) to evaporate on the substrate. We determined that PLL did not affect the minimum T_n (410 °C) and T_g (350 °C) required for straight [111]B-oriented growth. PLL treatment was used in all of the experiments reported here to prevent agglomeration of nanoparticles during deposition and to achieve an even nanoparticle distribution on the substrate.

Straight [111]B-oriented nanowires obtained at low growth temperature, made possible by the two-temperature procedure, were minimally tapered. The reduction in tapering is quantified in Figure 2a, which plots nanowire diameter measured at various distances from the Au-capped nanowire tip, for various T_g. These measurements were obtained from FESEM images of nanowires transferred to Si substrates. Ten nanowires were examined for each growth temperature. Only the upper section of the nanowires was examined because nanowire base growth is influenced, albeit minimally, by the brief high-temperature nucleation and cooling steps. Nanowire tapering is expressed in Table 1 as the increase in nanowire diameter (nm) per unit nanowire length (μm) from the Au nanoparticle−nanowire interface: Δ(diameter)/Δ(length) [nm/μm]. These data were calculated from the slopes of straight lines fitted to the data of Figure 2a.

The temperature-dependent reduction in tapering is explained with reference to the axial and radial growth mechanisms,[8,21] illustrated schematically in Figure 2b. Reaction species which impinge directly upon the nanoparticle contribute to axial growth. Additionally, Ga adatoms are adsorbed on the substrate and nanowire sidewalls and diffuse along the concentration gradient toward the growing nanoparticle−nanowire interface. These diffusing adatoms contribute to both radial and axial growth, hence radial growth competes with axial growth. Because radial growth is kinetically limited, diffusing adatoms are less likely to be incorporated into nanowire sidewalls at lower growth temperatures. Furthermore, adatom diffusion length decreases with decreasing growth temperature. This reduces the flux of adatoms diffusing from the substrate, limiting radial growth and tapering.

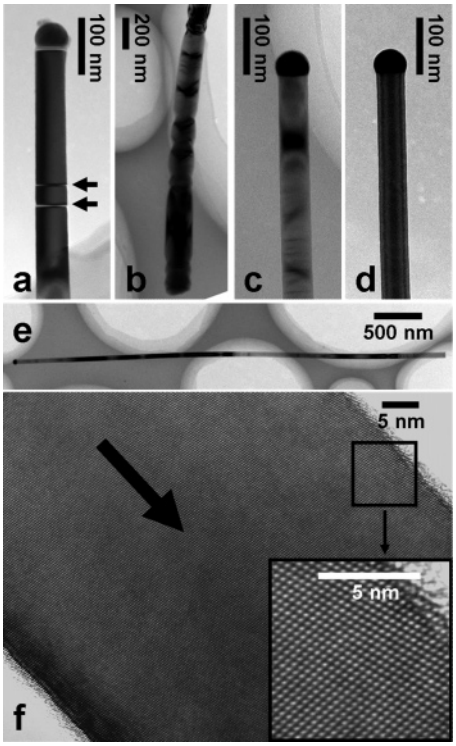

Figure 3. (a−e) Bright-field TEM and (f) HRTEM images showing morphologies and crystallographic quality of GaAs nanowires. (a, b) Nanowires grown at a high T_g of 450 °C by the single-temperature procedure, showing Au nanoparticle-capped nanowire tip with arrows labeling twin defects (a) and surface faceting toward the nanowire base (b). (c−f) Nanowires grown at a low T_g of 390 °C by the two-temperature procedure (T_n of 450 °C), showing nanowire tips (c and d), an entire nanowire (e), and a section of a nanowire (f). There are no lattice defects in (c) and (d), where the contrast in GaAs sections is due to bend contours (c) and thickness effects (d). The thick arrow in (f) indicates the nanowire growth direction.

We now characterize the crystallographic quality of these nanowires. All nanowires were of zinc blende structure. It has been well documented that crystallographic twins are common lattice defects in GaAs nanowires,[22] possibly because very little energy is required for twin formation.[23] Our extensive TEM investigation confirmed that twins, indeed, exist in the nanowires grown at a high T_g of 450 °C by the single-temperature procedure. Typical images of nanowire tip and base are shown in Figure 3a and b, respectively. In marked contrast, we cannot find any twins or other planar defects in nanowires grown at the lower T_g of 390 °C by the two-temperature procedure. Parts c and d of Figure 3 show nanowire tips, and Figure 3e illustrates an entire nanowire grown under these low-temperature conditions. This result is consistent with recent TEM studies of zinc blende GaP nanowires, which showed a distinct reduction in twin density with decreasing growth temperature.[11] Figure 3f shows high-resolution TEM (HRTEM) images, detailing the high crystallographic quality of a nanowire

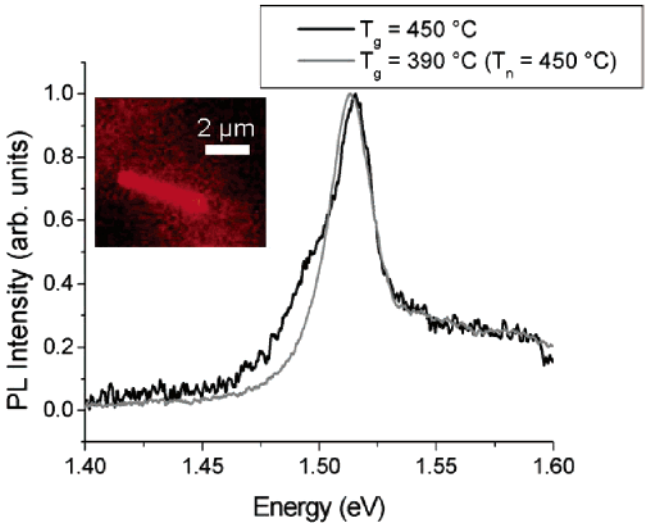

Figure 4. Normalized 10 K PL spectra of GaAs−AlGaAs core−shell nanowires for two different T_g. GaAs cores were grown at a T_g of 450 °C by the single-temperature procedure (black line). GaAs cores were grown at a T_g of 390 °C by the two-temperature procedure with a T_n of 450 °C (gray line). Inset: Room-temperature micro-PL image of the latter type of nanowire.

segment grown at the lower T_g of 390 °C by the two-temperature procedure. GaAs nanowires free of planar defects have previously been achieved growing in the [111]A direction on (111)A substrates, however, these [111]A-nanowires showed significant tapering and their growth orientation was less well-controlled than the nanowires reported here.[20]

Twin defects are closely associated with the sidewall faceting behavior of both zinc blende GaP[11] and GaAs nanowires.[24,25] Figure 3b illustrates the nonperiodic sawtooth faceted sidewalls and segmented appearance, typical of nanowires grown at high T_g (by the single-temperature procedure). The faceting occurs in association with the high density of twins in these nanowires: at least one twin defect is associated with the concave facet of each sawtooth and with each boundary between adjacent segments.[24] Radial growth augments the appearance of sidewall facets.[24] Nanowires grown at lower T_g (by the two-temperature procedure), as illustrated in Figure 3c−f, exhibit substantially smoother sidewalls. This is related to the elimination of twins and also to the reduction of radial growth.

PL spectra from ensembles of GaAs−AlGaAs core−shell nanowires are plotted in Figure 4. Nanowire GaAs cores were grown at the higher T_g of 450 °C by the single-temperature procedure, and the lower T_g of 390 °C by the two-temperature procedure. Both samples exhibit the same single broad peak at approximately 1.515 eV. This is consistent with previous measurements on single GaAs nanowires and corresponds closely to excitonic emission in bulk GaAs.[16] The high-energy shoulder is attributed to radiative recombination within AlGaAs portions of the nanowire. It indicates a nonuniform Al distribution with a lower Al composition than predicted from the vapor Al:Ga composition, in agreement with previous observations of AlGaAs nanowires and shells.[15,26]

The inset of Figure 4 shows a room-temperature micro-PL image of an individual two-temperature grown nanowire (T_g of 390 °C). PL from high-temperature grown (T_g of 450 °C) nanowires was too weak to be imaged successfully. This indicates that nanowires grown at low temperatures, made possible by the two-temperature process, have superior optical properties to their high-temperature grown counterparts. Improved PL emission is unexpected if we consider the smaller GaAs volume of the thin untapered low-temperature grown nanowire. Three factors could contribute to the observed PL enhancement. First, the low growth temperature eliminates twinning defects, which are believed to adversely affect the optical and electronic properties of the high-temperature grown nanowires.[16] Second, the low growth temperature reduces radial overgrowth, which is suspected to be of poor optical quality and may quench photoluminescence. Finally, the irregular facetted sidewalls of nanowires grown at high temperatures (Figure 3b) may cause roughness at the interface between the GaAs core and AlGaAs shell, resulting in a nonradiative recombination pathway. In contrast, the two-temperature grown nanowires exhibit very smooth sidewalls, leading to a smooth GaAs−AlGaAs interface that reduces nonradiative recombination.

The final question is why a high temperature ($T_n \geq$ 410 °C) is necessary to initiate straight epitaxial [111]B-oriented growth, which may then be maintained at a lower temperature ($T_g \geq$ 350 °C). The reasons are unclear, especially in light of recent debate regarding the state of the nanoparticle during growth, liquid or solid,[7,17,27] and whether adatoms are transported across the nanoparticle to the nanoparticle−nanowire interface by a liquid-phase, solid-phase, or surface diffusion mechanism.[27,28] Adhikari et al.,[13] in studies of two-temperature growth of Ge nanowires, propose a mechanism that assumes a liquid nanoparticle is necessary for epitaxial growth. According to this mechanism, Gibbs−Thomson pressure acts on the Ge nanowire due to its surface curvature but not on the Ge bulk, so that the nanoparticle−nanowire eutectic temperature is lower than the nanoparticle−bulk eutectic temperature. If this mechanism is correct, then higher initial temperatures serve to melt the nanoparticle in contact with the substrate and promote epitaxial nucleation. Once nanowire growth has initiated, a lower temperature can maintain the liquid nanoparticle and epitaxial growth.

For the Au−GaAs system under study, we devise a simple test for this Gibbs−Thomson pressure argument. Nanowire growth was initiated as described earlier by the two-temperature procedure with T_n of 450 °C and T_g between 350 and 390 °C. After several minutes of growth at T_g, TMG was removed, the sample was cooled to 200 °C, then reheated to the initial T_g, and TMG reintroduced to resume growth. This growth interruption is not expected to change the curvatures of the nanoparticle and nanowire significantly, so according to the Gibbs−Thomson pressure argument, epitaxial [111]B-oriented nanowire growth should resume. In contrast, nanowire growth consistently reinitiated in a kinked and irregular fashion at the point corresponding to the growth interrupt. We conclude that, although the Gibbs−

Thomson effect may contribute, it cannot completely describe our Au−GaAs system. We propose two alternative mechanisms below. The two mechanisms are not mutually exclusive, and both may play a role.

The first mechanism does not require any assumptions about the liquid or solid nature of the nanoparticle. This mechanism concerns the specific nanoparticle−GaAs interface conditions that are required for the nucleation and continuation of [111]B-oriented nanowire growth. We propose that the pregrowth annealing step is not sufficient to create these interface conditions. Instead, the interface is established at growth initiation when Ga adatoms are supplied, at or above the minimum T_n. This is reasonable given the sensitivity of GaAs (111)B surface reconstructions to temperature, Ga fluxes, and As fluxes.[29] Compositional changes within the nanoparticle, which occur when Ga adatoms are supplied, could also affect this interface. The minimum T_n represents the critical temperature required to reorder the substrate surface to remove surface roughness and to establish a planar nanoparticle−substrate interface. Once this interface is established, it is continuously regenerated as nanowire growth continues. Thus, the necessary interface conditions may be subsequently maintained at a lower temperature, down to the minimum T_g of 350 °C. Unless the interface conditions are established at the beginning of growth, the nanowires will not initiate in the [111]B direction. It is unlikely that these interface conditions will be established later on, explaining why nanowires that initially grow in nonvertical directions tend to undergo further kinking.

For the second mechanism, we note that, in the temperature range studied, the Au−Ga nanoparticle may be homogeneously liquid, homogeneously solid,[17] or may be inhomogeneous with Au−Ga crystalline phases existing in equilibrium with the liquid phase.[30] The presence of a solid phase could cause unstable kinked growth,[30] possibly because it hinders adatom diffusion and uniform deposition at the growing interface. We propose that a liquid nanoparticle is necessary for the initiation and continuation of epitaxial nanowire growth and that the nanoparticle experiences a temperature hysteresis between melting and solidification. This hysteresis has been observed by Tchernycheva et al. in reflection high-energy electron diffraction studies of the Au nanoparticle−GaAs bulk system[30] and Kofman et al. in studies of other metallic nanoparticles.[31] Further, the high AsH_3 pressure provided during pregrowth annealing is thought to limit the decomposition of the GaAs surface in contact with the Au nanoparticle,[17] comparable to a closed Au−GaAs system.[32] Thus, the Ga-rich eutectic liquid nanoparticle forms when TMG is supplied at growth initiation,[17] rather than during annealing, and the minimum T_n (410 °C) corresponds to the melting temperature. After melting, the liquid nanoparticle can be supercooled below this melting temperature until solidification at the minimum T_g (350 °C). Interestingly, we observe a 60 °C difference between the minimum T_n and the minimum T_g, very similar to the difference between melting and solidification temperatures observed by Tchernycheva et al.[30] We do not make inferences about the true nanoparticle temperature because the nominal thermocouple readings are a few tens of degrees above the true substrate temperature.

Both mechanisms state that the conditions (interface conditions, surface conditions, or liquid nanoparticle state) for stable [111]B-oriented growth are established at growth initiation rather than during pregrowth annealing. We tested this proposition in additional growth experiments that omitted this pregrowth annealing step. Straight [111]B-oriented nanowires were obtained with the same minimum T_n and T_g, regardless of whether annealing was performed or omitted. This supports the proposition that growth initiation above T_n, not annealing, produces the conditions required for epitaxial [111]B-oriented nanowires.

In summary, the two-temperature growth procedure produces straight, epitaxial [111]B-oriented GaAs nanowires at significantly lower growth temperatures than achieved previously. The lower growth temperature has significant advantages, namely the minimization of undesirable radial growth, elimination of twinning defects, and enhancement of nanowire optical quality. A low growth temperature will also limit the adatom diffusion distance along the (111)B substrate, thus minimizing any density dependencies of nanowire composition and height.[10] This procedure should enable the development of ternary nanowires with uniform composition and shape, and axial nanowire heterostructures free of undesirable shell overgrowth. It will therefore be beneficial not only for GaAs nanowires but also for other III−V nanowires.

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